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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,742	11/09/2001	Jun Koyama	740756-2384	5965

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EXAMINER

ECKERT II, GEORGE C

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 12/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/986,742

Applicant(s)

Koyama

Examiner

George C. Eckert II

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Nov 9, 2001
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on Nov 9, 2001 is/are a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 3-5 6) ☐ Other:

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DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figures 5-10, 15 and 18 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: on page 3, line 25, it is not clear what is meant by "influence of round of a signal[.]"

Appropriate correction is required.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

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Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,365,875 to Asai et al. Asai et al. teach, with reference to column 8 lines 18-43, a semiconductor device comprising:

a thin film transistor (e.g. figure 7(g)) comprising a polycrystalline semiconductor layer (e.g. 14, figure 7(d), col. 7, lines 46-49),

wherein a gate length of the thin film transistor is 10 μm (greater than 7 μm) and the gate width is 50 μm (col. 8, line 29).

The limitations that the transistor is used in a buffer circuit or a lcd based device are considered an intended use of the transistor structure and do not serve to further limit the structure of the instant claims. Moreover, Asai et al. teach that the transistor may be used in liquid crystal panels or contact type image sensors (col. 1, lines 13-16).

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Claim Rejections --35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. in view of US 6,090,650 to Dabral et al. Asai et al. teach a transistor in which the gate length is longer than 7 μm and the gate width is 50 μm (see Asai et al., col. 8, line 29). However, Asai et al. do not teach that the device is a multi-gate type device. Dabral et al. teach, with reference to figure 2, a transistor in which the gate 200 has multiple legs 205 (see also col. 4, lines 36-38).

Asai et al. and Dabral et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Asai et al. as a multi-gate device as taught by Dabral et al. The motivation for doing so, as is taught by Dabral et al., is that the use of a multi-gate structure will reduce the affect of processing variations in like devices (col. 3, lines 6-8). Therefore, it would have been obvious to combine Asai et al. with Dabral et al. to obtain the invention of claims 7-14.

7. Claims 15, 16, 19, 20, 22, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art as shown in figure 5, in view of Asai et al. Applicant's

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prior art teaches the various circuit arrangements as instantly claimed including current mirror and differential circuits. However, the prior art does not teach that the circuits use transistors having a gate length of 7 μm or greater or a gate width of 50 μm or greater. Asai et al. teach a transistor having the claimed gate dimensions.

Applicant's prior art and Asai et al are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the transistors of Asai et al. in the device of Applicant's admitted prior art. The motivation for doing so, as it taught by Asai et al., is that transistors having such dimensions and formed as taught by Asai et al. have uniform crystallinity in the semiconductor layer (col. 2, lines 5-13). Therefore, it would have been obvious to combine Applicant's prior art with Asai et al. to obtain the invention of claims 15, 16, 19, 20, 22, 25 and 26.

8. Claims 17, 18, 21, 23, 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art in view of Asai et al. and further in view of Dabral et al. As discussed immediately above, Applicant's prior art and Asai et al. make obvious a device having the instantly claimed circuit configuration and transistor gate dimensions. However, it is not made obvious by either reference that the transistor have a multi-gate. Dabral et al. teach, with reference to figure 2, a transistor having a multi-gate.

Applicant's prior art and Asai et al. are combinable with Dabral et al. because they are from the same field of endeavor. At the time of the invention it would have been obvious to a

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person of ordinary skill in the art to further modify the device of Applicant's prior art and Asai et al. to have a multi-gate as taught by Dabral et al. The motivation for doing so, as is taught by Dabral et al., is that the use of a multi-gate structure will reduce the affect of processing variations in like devices (col. 3, lines 6-8). Therefore, it would have been obvious to combine Asai et al. with Dabral et al. to obtain the invention of claims 17, 18, 21, 23, 24, 27 and 28.

Conclusion


9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references teach transistors having gate dimensions similar to those claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GCE
December 23, 2002


GEORGE ECKERT
PRIMARY EXAMINER